

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1 to 43 (Canceled)

1 44. (Previously Presented) A single integrated circuit
2 comprising:
3 a first data processor including
4 a first program counter (2903) storing an address of a
5 next instruction,
6 a first opcode register (2911) storing a current
7 instruction,
8 first data processing units (2902, 2905, 2906, 2907,
9 2908, 2909, 2910) capable of data processing,
10 a first control logic (2904) connected to said opcode
11 register for control of said first data processing units
12 corresponding to said current instruction stored in said first
13 opcode register according to a first instruction set;
14 a second data processor including
15 a second program counter (3100) storing an address of a
16 next instruction,
17 a second opcode register (3105) storing a current
18 instruction,
19 second data processing units (3301, 3302, 3303, 3304)
20 capable of data processing,
21 a second control logic (3002) connected to said opcode
22 register for control of said second data processing units
23 corresponding said current instruction stored in said second
24 opcode register according to a second instruction set, said
25 second data processing units having a different mapping of

26 instructions to controlled operations than that of said first
27 instruction set; and
28 an external interface (11) connected to said first and second
29 data processors and adapted for connection to memory (15) external
30 to said single integrated circuit, said external interface forming
31 the only connection between said first and second data processors
32 and memory external to said single integrated circuit;
33 where said first and second data processors are capable of
34 independent operations on disjoint instructions and data sets.

Claim 45. (Canceled)

1 46. (Previously Presented) The single integrated circuit of
2 claim 44, wherein:
3 said first data processor further includes a first data
4 register file (2901) connected to said first data processing units
5 for temporarily storing data; and
6 said second data processor further includes a second data
7 register file (3300) connected to said second data processing units
8 for temporarily storing data.

1 47. (Previously Presented) The single integrated circuit of
2 claim 44, further comprising:
3 a first read/write memory connected to said first data
4 processor and to said second data processor, whereby said first
5 processor and said second data processor are each capable of
6 reading from and writing to said first read/write memory; and
7 a second read/write memory connected to said second data
8 processor, whereby said second data processor is capable of reading
9 from and writing to said second read/write memory and said first
10 data processor is not capable of either reading from or writing to
11 said second read/write memory.

Claim 48. (Canceled)

1 49. (Previously Presented) The single integrated circuit of
2 claim 44, wherein:
3 said first data processor is a digital signal processor (DSP);
4 and
5 said second data processor is a reduced instruction set
6 computer (RISC) processor.

Claims 50 and 51. (Canceled)

1 52. (Previously Presented) A single integrated circuit
2 comprising:
3 a first data processor including
4 a first program counter (2903) storing an address of a
5 next instruction,
6 a first opcode register (2911) storing a current
7 instruction,
8 first data processing units (2902, 2905, 2906, 2907,
9 2908, 2909, 2910) capable of data processing,
10 a first control logic (2904) connected to said opcode
11 register for control of said first data processing units
12 corresponding to said current instruction stored in said first
13 opcode register according to a first instruction set;
14 a first read/write memory connected to said first data
15 processor, whereby said first processor is capable of reading from
16 and writing to said first read/write memory;
17 a first instruction memory connected to said first data
18 processor storing instructions in said first instruction set, said
19 first data processor operating in accordance with instructions in

20 said first instruction set recalled from said first instruction
21 memory;
22 a second data processor including
23 a second program counter (3100) storing an address of a
24 next instruction,
25 a second opcode register (3105) storing a current
26 instruction,
27 second data processing units (3301, 3302, 3303, 3304)
28 capable of data processing,
29 a second control logic (3002) connected to said opcode
30 register for control of said second data processing units
31 corresponding said current instruction stored in said second
32 opcode register according to a second instruction set, said
33 second data processing units having a different mapping of
34 instructions to controlled operations than that of said first
35 instruction set;
36 a second read/write memory connected to said second data
37 processor, whereby said second processor is capable of reading from
38 and writing to said second read/write memory;
39 a second instruction memory connected to said second data
40 processor storing instructions in said second instruction set, said
41 second processor operating in accordance with instructions in said
42 second instruction set recalled from said second instruction
43 memory; and
44 an external interface (11) connected to said first and second
45 data processors and connectable to memory (15) external to said
46 single integrated circuit, said external interface forming the only
47 connection between said first and second data processors and memory
48 external to said single integrated circuit;
49 where said first and second data processors are capable of
50 independent operations on disjoint instructions and data sets.

1 53. (Previously Presented) The single integrated circuit of
2 claim 52, wherein:

3 said first data processor further includes a first data
4 register file (2901) connected to said first data processing units
5 for temporarily storing data; and

6 said second data processor further includes a second data
7 register file (3300) connected to said second data processing units
8 for temporarily storing data.

1 54. (Previously Presented) The single integrated circuit of
2 claim 52, wherein:

3 said first data processor is a digital signal processor (DSP);
4 and

5 said second data processor is a reduced instruction set
6 computer (RISC) processor.

Claims 55 and 56. (Canceled)

1 57. (Previously Presented) The single integrated circuit of
2 claim 47, wherein:

3 said first data processor is operable to generate a request
4 for data movement to or from said first read/write memory;

5 said second data processor is operable to generate a request
6 for data movement to or from said first read/write memory and for
7 data movement to or from said second read/write memory;

8 said external interface is operable to receive a request for
9 data movement from said first data processor and from said second
10 data processor and to move data responsive thereto.

1 58. (Previously Presented) The single integrated circuit of
2 claim 57, wherein:

3 each request for data movement generated by said first data
4 processor or generated by said second data processor includes an
5 indication of source address, an indication of destination address
6 and an indication of amount of data; and
7 said external interface is operable upon receipt of said
8 request for data movement to move said indicated amount of data
9 from said indicated source address to said indicated destination
10 address.

1 59. (Previously Presented) The single integrated circuit of
2 claim 57, wherein:
3 said first read/write memory is operable to prioritize
4 requests for access with said first data processor having a highest
5 priority, said second data processor having an intermediate
6 priority and said external interface having a lowest priority.

1 60. (Previously Presented) The single integrated circuit of
2 claim 52, wherein:
3 said first data processor is operable to generate a request
4 for data movement to or from said first read/write memory;
5 said second data processor is operable to generate a request
6 for data movement to or from said first read/write memory and for
7 data movement to or from said second read/write memory;
8 said external interface is operable to receive a request for
9 data movement from said first data processor and from said second
10 data processor and to move data responsive thereto.

1 61. (Previously Presented) The single integrated circuit of
2 claim 60, wherein:
3 each request for data movement generated by said first data
4 processor or generated by said second data processor includes an

5 indication of source address, an indication of destination address
6 and an indication of amount of data; and
7 said external interface is operable upon receipt of said
8 request for data movement to move said indicated amount of data
9 from said indicated source address to said indicated destination
10 address.

1 62. (Previously Presented) The single integrated circuit of
2 claim 57, wherein:

3 said first read/write memory is operable to prioritize
4 requests for access with said first data processor having a highest
5 priority, said second data processor having an intermediate
6 priority and said external interface having a lowest priority.

1 63. (Previously Presented) A single integrated circuit
2 comprising:

3 a first data processor including
4 a first program counter (2903) storing an address of a
5 next instruction,
6 a first opcode register (2911) storing a current
7 instruction,
8 first data processing units (2902, 2905, 2906, 2907,
9 2908, 2909, 2910) capable of data processing,
10 a first control logic (2904) connected to said opcode
11 register for control of said first data processing units
12 corresponding to said current instruction stored in said first
13 opcode register according to a first instruction set;
14 a second data processor including
15 a second program counter (3100) storing an address of a
16 next instruction,
17 a second opcode register (3105) storing a current
18 instruction,

19 second data processing units (3301, 3302, 3303, 3304)
20 capable of data processing,
21 a second control logic (3002) connected to said opcode
22 register for control of said second data processing units
23 corresponding said current instruction stored in said second
24 opcode register according to a second instruction set, said
25 second instruction set units having a different mapping of
26 instructions to controlled operations than that of said first
27 instruction set;
28 a read/write memory connected to said first data processor and
29 said second data processor whereby both said first data processor
30 and said second data processor are each capable of reading from and
31 writing to said read/write memory;
32 an external interface (11) connected to said first data
33 processor, said second data processors and adapted for connection
34 to memory (15) external to said single integrated circuit, said
35 external interface forming the only connection between said first
36 data processor and said second data processors and memory external
37 to said single integrated circuit, wherein said first data
38 processor and said second data processor are each capable of
39 generating a request for data movement to or from said read/write
40 memory and said external interface is operable to receive a request
41 for data movement from said first data processor and from said
42 second data processor and to move data responsive thereto; and
43 wherein said first and second data processors are capable of
44 independent operations on disjoint instructions and data sets.

1 64. (Previously Presented) The single integrated circuit of
2 claim 63, wherein:

3 said first data processor further includes a first data
4 register file (2901) connected to said first data processing units
5 for temporarily storing data; and

6 said second data processor further includes a second data
7 register file (3300) connected to said second data processing units
8 for temporarily storing data.

1 65. (Previously Presented) The single integrated circuit of
2 claim 63, wherein:

3 each request for data movement generated by said first data
4 processor or generated by said second data processor includes an
5 indication of source address, an indication of destination address
6 and an indication of amount of data; and

7 said external interface is operable upon receipt of said
8 request for data movement to move said indicated amount of data
9 from said indicated source address to said indicated destination
10 address.

1 66. (Previously Presented) The single integrated circuit of
2 claim 63, wherein:

3 said read/write memory is operable to prioritize requests for
4 access with said first data processor having a highest priority,
5 said second data processor having an intermediate priority and said
6 external interface having a lowest priority.

1 67. (Previously Presented) The single integrated circuit of
2 claim 63, further comprising:

3 a second read/write memory connected to said second data
4 processor, whereby said second data processor is capable of reading
5 from and writing to said second read/write memory and said first
6 data processor is not capable of either reading from or writing to
7 said second read/write memory.

1 68. (Previously Presented) The single integrated circuit of
2 claim 63, wherein:

3 said first data processor is a digital signal processor (DSP);
4 and
5 said second data processor is a reduced instruction set
6 computer (RISC) processor.

1 69. (Previously Presented) A single integrated circuit
2 comprising:
3 a first data processor including
4 a first program counter (2903) storing an address of a
5 next instruction,
6 a first opcode register (2911) storing a current
7 instruction,
8 first data processing units (2902, 2905, 2906, 2907,
9 2908, 2909, 2910) capable of data processing,
10 a first control logic (2904) connected to said opcode
11 register for control of said first data processing units
12 corresponding to said current instruction stored in said first
13 opcode register according to a first instruction set;
14 a first read/write instruction memory connected to said first
15 data processor storing instructions in said first instruction set,
16 said first data processor operating in accordance with instructions
17 in said first instruction set recalled from said first instruction
18 memory;
19 a second data processor including
20 a second program counter (3100) storing an address of a
21 next instruction,
22 a second opcode register (3105) storing a current
23 instruction,
24 second data processing units (3301, 3302, 3303, 3304)
25 capable of data processing,
26 a second control logic (3002) connected to said opcode
27 register for control of said second data processing units

28 corresponding said current instruction stored in said second
29 opcode register according to a second instruction set, said
30 second data processing units having a different mapping of
31 instructions to controlled operations than that of said first
32 instruction set;
33 a second read/write instruction memory connected to said
34 second data processor storing instructions in said second
35 instruction set, said second processor operating in accordance with
36 instructions in said second instruction set recalled from said
37 second instruction memory; and
38 a read/write data memory connected to said first data
39 processor and said second data processor, whereby both said first
40 data processor and said second processor are capable of reading
41 from and writing to said read/write data memory.

1 70. (Previously Presented) The single integrated circuit of
2 claim 69, wherein:
3 said first data processor further includes a first data
4 register file (2901) connected to said first data processing units
5 for temporarily storing data; and
6 said second data processor further includes a second data
7 register file (3300) connected to said second data processing units
8 for temporarily storing data.

1 71. (Previously Presented) The single integrated circuit of
2 claim 69, wherein:
3 said read/write data memory is operable to prioritize requests
4 for access with said first data processor having a highest priority
5 and said second data processor having a lowest priority.

1 72. (Previously Presented) The single integrated circuit of
2 claim 69, further comprising:

3 a second read/write data memory connected to said second data
4 processor, whereby said second data processor is capable of reading
5 from and writing to said second read/write data memory and said
6 first data processor is not capable of either reading from or
7 writing to said second read/write data memory.

1 73. (Previously Presented) The single integrated circuit of
2 claim 69, wherein:

3 said first data processor is a digital signal processor (DSP);
4 and

5 said second data processor is a reduced instruction set
6 computer (RISC) processor.

1 74. (Previously Presented) The single integrated circuit of
2 claim 69, wherein:

3 said first and second data processors are capable of
4 independent operations on disjoint instructions and data sets.

1 75. (Previously Presented) The single integrated circuit of
2 claim 69, wherein:

3 said first read/write instruction memory being configured as a
4 first instruction cache;

5 said second read/write instruction memory being configured as
6 a second instruction cache;

7 said first data processor further including a first
8 instruction cache logic circuit (3101) connected to said program
9 counter and said first instruction cache for determining if an
10 instruction corresponding to the address stored in said first
11 program counter is stored in said first instruction cache;

12 said second data processor further including a second
13 instruction cache logic circuit connected to said second program
14 counter and said second instruction cache for determining if an

15 instruction corresponding to the address stored in said second
16 program counter is stored in said second instruction cache; and
17 an external interface (11) connected to said first data
18 processor, said second data processor, said first instruction cache
19 and said second instruction cache and connectable to memory (15)
20 external to said single integrated circuit, said external interface
21 transferring an instruction corresponding to the address stored in
22 said first program counter from said memory external to said single
23 integrated circuit to said first instruction cache if said first
24 instruction cache logic circuit determines said instruction is not
25 stored in said first instruction cache, and said external interface
26 transferring an instruction corresponding to the address stored in
27 said second program counter from said memory external to said
28 single integrated circuit to said second instruction cache if said
29 second instruction cache logic circuit determines the instruction
30 is not stored in said second instruction cache.